IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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|---|---|---|---|
| Applicant(s): | Adi Srinivasan | | |
| Assignee: | Sequence Design, Inc. | | |
| Title: | Circuit Optimization For Minimum Path Timing Violations | | |
| Serial No.: | Unassigned | Filing Date: | Herewith |
| Examiner: | Unknown | Group Art Unit: | Unassigned |
| Docket No.: | M-11985-1D US | | |

San Jose, California
July 25, 2003

Mail Stop Patent Application
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**PRELIMINARY AMENDMENT**

Dear Sir:

Prior to the calculation of fees, please make the following amendments to the above-referenced patent application as follows.